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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,910	07/23/2001	Yoshio Sano	Q65531	9164

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SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 Pennsylvania Avenue, N.W.,
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EXAMINER
DONG, DALEI

ART UNIT	PAPER NUMBER
2875	

DATE MAILED: 11/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/909,910	SANO ET AL.	
	Examiner	Art Unit	
	Dalei Dong	2875	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/909,910* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 21, 23, 26, 28, 31, 32, 35, 37, and 38-42 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,952,782 to Nanto.

Regarding to claims 1 and 37, Nanto discloses in Figure 1, a plasma display panel "having a three-electrode structure with a matrix display from that is called a reflection type. The external appearance is derived from paired glass substrates 11 and 21, which face each other with an intervening discharge space 30 therebetween. The glass

substrates 11 and 21 are bonded by a seal frame layer (not shown) of a glass having a low-melting point that is formed along the edges of the facing substrate" (column 5, line 39-46). Nanto also discloses, "a pair of display electrodes X and Y comprises a wide, linear transparent electrode 41 formed of ITO thin film and a narrow, linear bus electrode 42 formed of metal thin film having a multi-layer structure. As specific example sizes, the transparent electrode 41 is 0.1 μm thick and 180 μm wide, while the bus electrode 42 is 1 μm thick and 60 μm wide" (column 5, line 52-57). Nanto further discloses in Figure 6, "a width w47 of the light shielding film 47 is greater than a width w2 of the reverse slit S2, and is smaller than the interval w22 between the edges, which are closer to the discharge slit S1, of the metal electrodes 42 sandwiching the reverse slit S2" (column 8, line 57-61).

Regarding to claim 2, 3, 23, and 28, Nanto discloses in Figure 3, "the shielding films 45 are formed in patterns of belts that extend along the display lines, and are located to overlap areas sandwiched between the display electrodes X and Y of the adjacent lines L" (column 6 line66-67 to column 7, line 1-2). Nanto also discloses in Figure 4B, "an ITO film is deposited on the glass substrate 11, whereon the light shielding films 45 are formed, and patterning of the ITO film is performed by photolithography using a second light exposing mask. Transparent electrodes 41are thus formed so that they partially overlap the light shielding films 45" (column 7, line 37-42). The neighboring electrodes are connected electrically via the shielding film of Nanto.

Regarding to claim 4, the claim pertains to the method for fabricating the plasma display panel. As to the product-by-process limitation "encapsulating the substrates in a

vacuum" of claim 4, it has been recognized that "[E]ven though product-by-process claims are limited by and defined by the process, determination of patenability is based on the product by itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior art product was made by a different process". *In re Thrope*, 227 USPQ 964,996 (Fed. Cir. 1985). See also MPEP 2113.

Regarding to claim 5, Nanto discloses in Figure 1, "on the dielectric layer 24, a plurality of barrier ribs 29 which are about 150 μm high and linear in a plan view, are individually arranged between the address electrodes A" (column 6, line 21-23).

Regarding to claims 21 and 26, Nanto discloses, "Chromium oxide (CrO) or silicon oxide can be used as the insulation material. It is desirable that the thickness of the insulation film be 1 μm or less in order to reduce the step difference to the transparent electrodes 41. Then, patterning is performed to the insulation film by photolithography using a first light exposing mask, and a plurality of the light shielding film stripes 45 described above are produced at one time (Figure 4A)" (column 7, line 29-36).

Regarding to claims 31, 32, and 35, Nanto discloses "the size of a gap (the width of a reverse slit) for display lines L, along which the paried display electrodes X and Y are arranged, is set to from 100 μm to 400 μm, which is sufficiently large compared with the size of a surface discharge gap (the width of a discharge slit) of 50 μm for each display line L, the interference of a discharge does not occur between the lines L" (column 6, line 41-47).

Regarding to claims 38-42, Nanto discloses in Figure 3, "the shielding films 45 are formed in pattern of belts that extend along the display lines, and are located to overlap the areas sandwiched between the display electrodes X and Y of the adjacent lines L" (column 6, line 66-67 to column 7, line 1-2). Nanto also discloses "the top portions of the barrier ribs 29 have the same dark color as that of the light shielding films. A dark lattice pattern is formed by intersecting the barrier ribs and light shielding films, and the outline of each sub-pixel becomes clear" (column 7, line 11-15). Nanto further discloses "Chromium oxide (CrO) or silicon oxide can be used as the insulation material. It is desirable that the thickness of the insulation film be 1 μm or less in order to reduce the step difference to the transparent electrodes 41. Then, patterning is performed to the insulation film by photolithography using a first light exposing mask, and a plurality of the light shielding film stripes 45 described above are produced at one time (Figure 4A)" (column 7, line 29-36). Nanto further yet discloses in Figure 7, "it is important for the light shielding films 49 to overlap the electrodes X and Y up to around the middle portions of the bus electrodes 42, which constitute a three-layer structure of Cr/Cu/Cr. In other words, while the bus electrodes 42 provide a higher conductivity for a highly resistant material for the transparent electrodes 41, the electrodes 42 themselves possess light shielding property. When the light shielding films 49 are so formed that they overlap the bus electrodes 42, the portions, except for the display line areas L, are completely shielded" (column 9, line 16-26).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,952,782 to Nanto in view of U.S. Patent No. 5,557,168 to Nakajima.

Regarding to claims 6-7, Nanto discloses a plasma display panel comprising a front substrate, a rear substrate, a sealing portion for encapsulating the two substrates, column ribs and row ribs for defining pixel cells and an plane discharge electrodes. However, Nanto dose not disclose a gap between the top of rib and the front substrate; further a projected portion on the intersection of the lattice-shaped ribs. Nakajima teaches in Figure 3, "a spacer 28 of an insulating material like a glass is attached to the crossing of first second separating walls 26a and 26b" (column 4, line 44-46). Nakajima also teaches the "spacer 28 is between front barrier rib 26 and cathode support layer 22, a space 35 having the same height as spacer 28 is formed between first cylindrical cathode 20 and spacer 28. In discharge, ions can move between discharge cells 30 through space 35" (column 5, line 18-22). It would have been obvious to one of ordinary skills in the art at the time the invention was made to utilize the spacer of Nakajima between the lattice-shaped ribs and the front substrate of Nanto in order to provide a high optical-

output efficiency and high peak intensity and which can be driven with less maximum power consumption.

Regarding to claim 8, Nanto discloses a plasma display panel comprising a front substrate, a rear substrate, a sealing portion for encapsulating the two substrates, column ribs and row ribs for defining pixel cells and an plane discharge electrodes. However, Nanto dose not disclose the projected portion define the electrodes between pixel cells. Nakajima teaches in Figure 1, "cathode lead pattern 18 of rear substrate 12 and transparent anode 24 of front substrate 14 cross each other a predetermined distance apart, and each of first cylindrical cathode 20 is located corresponding discharge cell 30. Spacer 28 attached to front barrier rib 26 is in contact with the surface of cathode support layer 22. End 20b of first cylindrical cathode 20 faces belt-shaped transparent anode 24 a predetermined distance apart" (column 4, line 47-54). The spacer of Nakajima further functions as a "defining" component for the electrodes. It would have been obvious to one of ordinary skills in the art at the time the invention was made to utilize the spacers of Nakajima between the lattice-shaped rib and the front substrate of Nanto in order to further "define" the electrodes in the plasma display and also provide a high optical-output efficiency and high peak intensity and which can be driven with less maximum power consumption.

6. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,952,782 to Nanto in view of U.S. Patent No. 5,557,168 to Nakajima in further view of U.S. Patent No. 5,889,365, to Tanabe.

Regarding to claims 9 and 10, Nanto discloses a plasma display panel comprising a front substrate, a rear substrate, a sealing portion for encapsulating the two substrates, column ribs and row ribs for defining pixel cells and an plane discharge electrodes. However, Nanto dose not disclose a gap for allowing gas to pass through between the top of the lattice-shaped rib and the front substrate and a recessed portion provided on the intersections of lattice-shaped ribs, which define electrodes between pixel cells. Nakajima teaches a gap for allowing gas to pass through between the top of the lattice-shaped rib and the front substrate; however, Nakajima does not teach a recessed portion on the intersections of the lattice-shaped ribs. Tanabe teaches in Figure 2A and 2B a plasma display panel comprising "barrier ribs 27 are formed in the shape of a grid between the front plate 21 and the rear plate 22 to form a plurality of discharge cells 26." (column 3, line 48-50). Tanabe also teaches "the barrier ribs 27 are formed on an insulating layer 30 formed on the rear plate 22, fluorescent coating 31 of fluorescent materials are formed on inner surfaces of the barrier ribs 27, and the priming slits 32 are formed in the upper ends of the barrier ribs 27" (column 4, line 22-26). The priming slits or recessive portion of Tanabe are formed at the intersections of the lattice-shaped ribs; further the priming slits of Tanabe "define" the electrodes between pixel cells. It would have been obvious to one of ordinary skills in the art at the time the invention was made to utilize the priming slits or recessive portion of Tanabe at the intersection of the lattice-shaped ribs of Nanto which forms a gap between the lattice-shaped ribs and the front substrate in order to provide a high optical-output efficiency and high peak intensity and which can be driven with less maximum power consumption.

7. Claims 11-15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,952,782 to Nanto in view of U.S. Patent No. 5,557,168 to Nakajima in further view of U.S. Patent No. 5,939,828 to Matsuzaki.

Regarding to claims 11-15, Nanto discloses a plasma display panel comprising a front substrate, a rear substrate, a sealing portion for encapsulating the two substrates, column ribs and row ribs for defining pixel cells and an plane discharge electrodes. However, Nanto dose not disclose a gap for allowing gas to pass through between the top of the lattice-shaped rib and front substrate and a horizontal barrier wall formed of a material having a dielectric constant lower than the insulating layer; further the horizontal barrier wall comprising an extended portion. Nakajima teaches a gap for allowing gas to pass through between the top of the lattice-shaped rib and the front substrate; however, Nakajima does not teach a horizontal barrier wall formed of a material having a dielectric constant lower than the insulating layer and the horizontal barrier wall comprising an extended portion. Matsuzaki teaches in Figures 10(a) to 10 (c) a barrier wall 110 and also according to the Matsuzaki "the voltage applied to the address electrodes 10 for generating the address discharge and the voltage applied to the display electrodes 6 (or bus electrodes) is lowered, the height of the barrier rib 110 is not increased. For example, the height of the barrier ribs is from 0.15 to 0.02 mm in the standard gas discharge type display device, whereas the height is from 0.05 to 0.1 mm in this embodiment, which is less than ½ of that of the standard device" (column 19, line 16-24). Matsuzaki also teaches "the barrier ribs 110 forming the discharge space on the side of the front substrate

are formed by the partition wall substrate 90 comprising a metal plate having openings and covered with the insulation film" (column 10, line 39-44). The metal plate that forms the barrier wall has a lower dielectric constant than the insulating layer. As shown in the different embodiments of Matsuzaki the barrier wall is placed on one of the sustain electrode or the scan electrodes and the barrier wall have different widths for the two types of electrodes. Matsuzaki further teaches in Figure 17(a), 17(b) and Figure 18(a) "a branched portion is disposed on one side of the address electrodes 10 which protrudes toward the main discharging space 100 at locations where the display electrodes 62, acting as a common electrode in the main discharge for display, and the address electrodes 10 intersect. In this case, since the address electrodes 10 are formed on the barrier ribs 11, the barrier ribs also protrude in the discharging space 200. A portion showing the feature of this embodiment is depicted by 340 in Figure 18(a)" (column 27 line 65-67 to column 28 line 1-8). It would have been obvious to one of ordinary skills in the art at the time the invention was made to utilize the horizontal barrier wall of Matsuzaki in combination with the gap of Nakajima for the plasma display panel of Nanto in order to provide a high optical-output efficiency and high peak intensity and which can be driven with less maximum power consumption.

Regarding to claims 17-19, Nanto discloses a plasma display panel comprising a front substrate, a rear substrate, a sealing portion for encapsulating the two substrates, column ribs and row ribs for defining pixel cells and an plane discharge electrodes. However, Nanto dose not disclose a gap for allowing gas to pass through between the top of the lattice-shaped rib and the front substrate and further a horizontal barrier wall

located with respect to the bus electrode. Nakajima teaches a gap for allowing gas to pass through between the top of the lattice-shaped rib and the front substrate; however, Nakajima does not teach the location of the horizontal barrier wall with respect to the bus electrode. As shown in Figure 3(c) the bus electrodes 73 does not overlap the horizontal barrier wall 110 however it does overlap the barrier rib 11. As shown in Figure 1(a) to 1(c), the bus electrodes 71 and 72 overlap horizontal barrier wall 110 and not the barrier rib 11. Finally, as shown in Figure 7(a) to 7(c), the bus electrodes 71 and 72 overlap both the horizontal barrier wall 110 and the barrier rib 11. It would have been obvious to one of ordinary skills in the art at the time the invention was made to utilize the horizontal barrier wall location with respect to the bus electrodes in combination with the gap of Nakajima for the plasma display panel of Nanto in order to provide a high optical-output efficiency and high peak intensity and which can be driven with less maximum power consumption.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,952,782 to Nanto in view of U.S. Patent No. 5,557,168 to Nakajima in further view of U.S. Patent No. 6,008,582 to Asano.

Regarding to claim 16, Nanto discloses a plasma display panel comprising a front substrate, a rear substrate, a sealing portion for encapsulating the two substrates, column ribs and row ribs for defining pixel cells and an plane discharge electrodes. However, Nanto dose not disclose a gap for allowing gas to pass through between the top of the lattice-shaped rib and the front substrate; further Nanto dose not disclose the lattice-

shaped ribs having different height extending in different directions. Nakajima teaches a gap for allowing gas to pass through between the top of the lattice-shaped rib and the front substrate; however, Nakajima does not teach the lattice-shaped ribs having different height extending in different directions. Asano teaches in Figure 4 and 5 "a back plate 3 provided with a plurality of parallel partition walls, and auxiliary partition walls extended perpendicularly to the partition walls between the adjacent partition walls. In Figure 4, only the partition walls (barrier ribs) 1a, 1b and 1c among the plurality of partition walls, and only the partition walls 52a, 52b, 52c and 52d among the auxiliary partition walls are shown" (column 9, line 1-8). It would have been obvious to one of ordinary skills in the art at the time the invention was made to utilize the auxiliary partition wall of Asano in combination of the gap of Nakajima for the plasma display panel of Nanto in order to provide a high optical-output efficiency and high peak intensity and which can be driven with less maximum power consumption.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,952,782 to Nanto in view of U.S. Patent No. 5,557,168 to Nakajima in further view of U.S. Patent No.6,037,713 to Fukuta.

Regarding to claim 20, Nanto discloses a plasma display panel comprising a front substrate, a rear substrate, a sealing portion for encapsulating the two substrates, column ribs and row ribs for defining pixel cells and an plane discharge electrodes. However, Nanto dose not disclose a gap for allowing gas to pass through between the top of the lattice-shaped rib and the front substrate; further Nanto dose not disclose the thickness of

the bus electrode. Nakajima teaches a gap for allowing gas to pass through between the top of the lattice-shaped rib and the front substrate; however, Nakajima does not teach the thickness of the electrode. Fukuta teaches "the thickness of the aluminum electrodes is typically 5,000 Å to 40,000 Å for the bus electrodes in the PDP, 5,000 Å to 20,000 Å for the address electrodes in the PDP, and 500 Å 3,000 Å for the gate electrodes of the TFTs in the active matrix liquid crystal display device and for the scanning electrodes and the signal electrodes in the simple matrix liquid crystal display device" (column 5, line 5-11). It is also old and well known in the art that the thickness of the electrode can be adjusted in accordance with the resistance desired for the electrodes. It would have been obvious to one of ordinary skills in the art at the time the invention was made to utilize the aluminum bus electrodes of Fukuta along with the gas of Nakajima in the plasma display panel Nanto in order to provide a high optical-output efficiency and high peak intensity and which can be driven with less maximum power consumption.

10. Claims 22, 27, 33, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,952,782 to Nanto.

Regarding to claim 22 and 27, Nanto discloses in Figure 1, "display electrodes X and Y comprises a wide, linear transparent electrode 41" (column 5, line 52-53); further Nanto discloses "as shown in Figure 3, the shielding films 45 are formed in patterns of belts that extend along the display lines and are located to overlap the areas sandwiched between the display electrodes X and Y" (column 6, line 66-67 to column 7 line 1). It would have been obvious to one of ordinary skills in the art at the time the invention was

made to have made the light shielding film of Nanto transparent in order to provide a high optical-output efficiency and high peak intensity and high optical –output luminescence and which can be driven with less maximum power consumption.

Regarding to claims 33 and 34, Nanto discloses in Figure 6, "a light shielding film 47 is provided for each reverse slit S2 in an intermediate portion in the direction of the thickness of a dielectric layer 17. The light shielding film 47, as well as the light shielding films 45 in Figure 3, are extended in a belt shape along the display line in a plan view, and constitute a striped light shielding pattern" (column 8, line 50-56). The light shielding film of Nanto is composite of chromium oxide, a type of metal that may be used to compose electrode. It would have been obvious to one of ordinary skills in the art at the time the invention was made to utilize the metal light shielding film of Nanto as a scan-electrode in order to provide a high optical-output efficiency and high peak intensity and high optical –output luminescence and which can be driven with less maximum power consumption.

11. Claims 24 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,952,782 to Nanto in view of U.S. Patent No. 5,900,694 to Matsuzaki.

Regarding to claims 24 and 29, Nanto discloses a plasma display panel comprising a front substrate, a rear substrate, a sealing portion for encapsulating the two substrates, column ribs and row ribs for defining pixel cells and an plane discharge electrodes and also a metal electrode connecting the two electrodes. However, Nanto dose not disclose the resistance of the common bus electrode is 1/3 to 1/12 of the scan-

side bus electrode. Matsuzaki teaches in Figure 25a, "the bus electrode 62 and 72 have branchlike members 18b, so that the resistance thereof is lower than that of the bus electrodes of the conventional display panel having no branchlike member" (column 3, line 49-52). Matsuzaki also teaches in Figure 6a to 6c, the bus electrode 192 of the central main discharge electrode 19 among the three main discharge electrodes 6 and 19 has branchlike member 18b on both sides, and the bus electrodes 62 of the other main discharge electrodes 6 are arranged so that the sides thereof on which the branchlike members 18b are provided face the central main discharge electrode 7" (column 9, line 1-8). The bus electrodes of Matsuzaki have a resistance difference of 1/3 to 1/12 proportionally. It would have been obvious to one of ordinary skills in the art at the time the invention was made to utilize the different resistance bus electrodes of Matsuzaki for the plasma display panel of Nanto in order to provide a high optical-output efficiency and high peak intensity and which can be driven with less maximum power consumption.

12. Claims 25 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No.5,952,782 to Nanto in view of U.S. Patent No. 6,037,713 to Fukuta.

Regarding to claims 25 and 30, Nanto discloses a plasma display panel comprising a front substrate, a rear substrate, a sealing portion for encapsulating the two substrates, column ribs and row ribs for defining pixel cells and an plane discharge electrodes and also a metal electrode connecting the two electrodes. However, Nanto dose not disclose the bus electrode has a thickness of 10 to 50 μm. Fukuta teaches "the thickness of the aluminum electrodes is typically 5,000 Å to 40,000 Å for the bus

electrodes in the PDP, 5,000 Å to 20,000 Å for the address electrodes in the PDP, and 500 Å 3,000 Å for the gate electrodes of the TFTs in the active matrix liquid crystal display device and for the scanning electrodes and the signal electrodes in the simple matrix liquid crystal display device" (column 5, line 5-11). It would have been obvious to one of ordinary skills in the art at the time the invention was made to utilize the bus electrode of Fukuta in the plasma display panel of Nanto in order to provide a high optical-output efficiency and high peak intensity and which can be driven with less maximum power consumption.

13. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,952,782 to Nanto in view U.S. Patent No. 4,629,942 to Horio.

Regarding to claim 36, Nanto discloses a plasma display panel comprising a front substrate, a rear substrate, a sealing portion for encapsulating the two substrates, column ribs and row ribs for defining pixel cells. However, Nanto does not disclose the electrode has a portion reduced in width. Horio teaches "as specifically identified in Figure 8, therefore, the segmented, first driving electrode 54-1 includes a segment of normal width overlying the corresponding uppermost coupling electrode 51a in each of the three successive groups thereof, but is narrowed in the regions 55a and 55b which cross over the interconnections 19 formed on the underlying substrate21" (column 16, line 35-41). It would have been obvious to one of ordinary skills in the art at the time the invention was made to utilize the different width electrode of Horio for the plasma display panel of

Nanto in order to provide a high optical-output efficiency and high peak intensity and which can be driven with less maximum power consumption.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following cited patents are cited to further show the state of the art with respect to the plasma display panel.

U.S. Patent No. 5,701,056 to Shinohara.

U.S. Patent No. 5,744,909 to Amano.

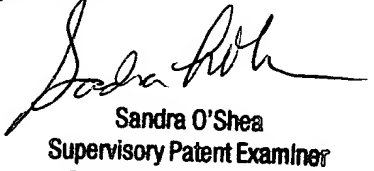
U.S. Patent No. 5,982,095 to Jin.

U.S. Patent No. 6,088,011 to Lee.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dalei Dong whose telephone number is (703)308-2870. The examiner can normally be reached on 8 A.M. to 5 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sandra O'Shea can be reached on (703)305-4939. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.



Sandra O'Shea
Supervisory Patent Examiner
Technology Center 2800

D.D.
October 29, 2002